AP

Docket No.: 50099-184 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Masato FUJINAGA	:	Confirmation Number: 1996
Application No.: 09/977,274	:	Tech Center Art Unit: 2826
Filed: October 16, 2001	:	Examiner: Leonardo Andujar

For: HIGH-FREQUENCY SEMICONDUCTOR DEVICE WITH NOISE ELIMINATION CHARACTERISTIC (AS AMENDED)

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellant's Appeal Brief in support of the Notice of Appeal filed December 10, 2004. Please charge the Appeal Brief fee of $500.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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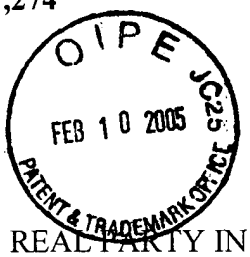

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APPEAL BRIEF

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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed December 10, 2004, wherein Appellant appeals from the Primary Examiner's rejection of claims 18-21, 23 and 24.

I. Real Party In Interest

The real party in interest in this application are the assignees, Renesas Technology Corporation and Renesas LSI Design Corporation.

II. Related Appeals and Interferences

Appellant is unaware of any related Appeal or Interference.

III. Status of Claims

Claims 18-21, 23 and 24 stand twice rejected and are subject to this Appeal. Claims 1-8 and 17 were previously canceled and claims 9-16 were withdrawn from consideration pursuant to a previous restriction requirement. Claim 22 was objected to and indicated as allowable subject matter, if rewritten in independent form.

IV. Status of Amendments

No amendment has been filed since the final rejection dated October 10, 2004. Hence, there is no outstanding amendment that has not been entered.

V. Summary of Claimed Subject Matter

The present claimed subject matter relates to a high-frequency semiconductor device capable of implementing an enhancement in a noise eliminating characteristic of a wiring (page 3 of the specification, lines 1 through 2). The present invention addresses and solves problems and difficulties in the prior art by providing a first wiring that is continuously covered by a conductor layer with an insulator interposed therebetween in a section crossing a direction of extension of the first wiring (page 9 of the specification, lines 11 through 13). By using the conductor layer as a power line (including a grounding conductor), it is possible to reduce a noise entering in and emitted from the first wiring than compared to a conventional device (page 9 of the specification, lines 13 through 16). Further, the conductor layer can be formed to bury the first wiring therein (page 9 of the specification, lines 16 through 17). As illustrated in Figure 1 of the present disclosure, a grounding conductor layer includes a single unit first portion 19 covering the upper surface and two side surfaces of the first wiring 15 and the second portion 12 covering the

bottom surface of the first wiring 15. With the structure of the present device, it is possible to achieve an enhancement in noise eliminating characteristics of the wiring compatibly with promotion of microfabrication and the simplification of the manufacturing process (page 9 of the specification, lines 20 through 22).

Independent claim 18 describes a high-frequency semiconductor device. The semiconductor device 101 comprises a semiconductor substrate 1 having a main surface. A first wiring 15 provided over the main surface of the semiconductor substrate 1. A grounding conductor layer continuously covers a periphery of the first wiring 15 with a first insulator 14 interposed therebetween in a section crossing a direction of extension of the first wiring 15. The grounding conductor layer transmits a grounding potential and includes a first portion 19 constituted by only one unit covering an upper surface and two side surfaces of the first wiring 15 and a second portion 12 covering a bottom surface of the first wiring 15.

VI. Grounds of Rejection To Be Reviewed By Appeal

The Rejections:

1. Claims 18, 20 and 24 were rejected under 35 U.S.C. § 102(b) for lack of novelty as evidenced by Korean Patent Application Laid-Open No. 1999-73868; and

2. Claims 19, 21 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over by Korean Patent Application Laid-Open No. 1999-73868.

The Issues Which Arise In This Appeal and Require Resolution by the Honorable Board of Patent Appeals and Interferences are:

1. Whether claims 18, 20 and 24 are unpatentable under 35 U.S.C. § 102 for lack of novelty as evidenced by Korean Patent Application Laid-Open No. 1999-73868; and

2. Whether claims 19, 21 and 23 are unpatentable under 35 U.S.C. §103 for obviousness predicated upon Korean Patent Application Laid-Open No. 1999-73868.

VII. Argument

Issue 1 - The rejection of claims 18, 20 and 24 under 35 U.S.C. § 102 for lack of novelty as evidenced by Korean Patent Application Laid-Open No. 1999-73868

Examiner's Position

In the statement of the rejection (page 2 of the October 10, 2004 Office Action, hereinafter "Office Action"), the Examiner referred to Fig. 3 of KR 1999-73868, asserting the disclosure of a semiconductor device corresponding to that defined in independent claim 18 and dependent claims 20 and 24. The Examiner, at page 3 of the Office action, asserted that KR 1999-73868 discloses a grounding conductor layer including a first portion 116 covering an upper surface and two side surfaces of a first wiring 108 and a second potion 112 covering a bottom surface of the wiring 108. The Examiner, in referencing page 2, line 1 of the partial English translation of KR 1999-73868, asserted that the reference refers to element 116 as a "first noise shielding film". The Examiner has interpreted the first noise shielding film 116 as being constituted by only one unit. Further, the Examiner, on page 5 of the Office action, relied on the dictionary definition of unit as being "a group, a structure or functional constituent of a whole."

Appellant's Position

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention under any statutory provision always rests upon the Examiner. *In re Mayne*, 41 USPQ2d 1451 (Fed. Cir. 1997); *In re Duel*, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Bell*, 26 USPQ2d 1529 (Fed. Cir. 1993). Appellant submits that this burden has not been established.

Independent claim 18 recites, in pertinent part, that the grounding conductor layer continuously covers a periphery of the first wiring with a first insulator interposed therebetween and the grounding conductor layer includes a first portion constituted by only one unit covering an upper surface and two side surfaces of the first wiring and a second portion covering a bottom surface of the first wiring. In contrast, KR 1999-73868 discloses a grounding conductor layer 116 that includes multiple units, 116a and 116b, which cover an upper surface and two side surfaces of a first wiring 108; and a second potion 112 covering a bottom surface of the wiring 108. The present claimed invention, as recited in claim 18, requires that the grounding conductor layer includes a first portion constituted by only one unit covering an upper surface and two side surfaces of the first wiring and a second portion covering a bottom surface of the first wiring. As depicted in Figure 1 of the present disclosure, the grounding conductor layer includes a single unit first portion 19 covering the upper surface and two side surfaces of the first wiring 15 and the second portion 12 covering the bottom surface of the first wiring. As clearly illustrated in Fig. 3 of KR 1999-73868, the upper surface of the first wiring 108 is covered with the conductor layer 116b, and two side surfaces of the first wiring 108 are covered with the conductor layer 116a. In other words, the upper surface and the two side surfaces of the first wiring 108 are covered not with a single conductor layer, but with two conductor layers (units) 116a and 116b, as evidenced by the separating line shown in Figure 3 of the reference.

Appellant submits that the present claim language in view of the specification, as well as Appellant's arguments, clearly distinguish the present invention over KR 1999-73868. The scope of protection defined (in part) by claim 18, when reasonably interpreted in light of and consistent with the supporting specification, encompasses a first portion constituted by only one unit (a single, individual portion) and does not include a multiple unit or grouping as described in KR 1999-73868. The Court of Appeals for the Federal Circuit has held that the claim limitation "single piece construction" does not include a "multiple piece construction". *W.E. Hall Co. v. Atlanta Corrugating, LLC*, 370 F.3d 1343, 71 USPQ2d 1135 (Fed. Cir. 2004). Therefore, significance must be accorded the claim requirement of only a single unit.

Accordingly, KR 1999-73868 fails to identically disclose every feature recited in independent claim 18 as required for a tenable rejection under 35 U.S.C. § 102(2). The reference simply does not disclose a single unit configured as recited in claim 18. The above argued structural difference between the claimed invention and the device of KR 1999-73868 undermine the factual determination that KR 1999-73868 discloses a semiconductor device identically corresponding to those claimed. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Appellant, therefore, submits that the imposed rejection of claims 18, 20 and 24 under 35 U.S.C. § 102 for lack of novelty as evidenced by KR 1999-73868 is not factually viable and, hence, solicit reversal thereof.

Issue 2 - The rejection of dependent claims 19, 21 and 23 under 35 U.S.C. §103 for obviousness predicated upon Korean Patent Application Laid-Open No. 1999-73868

Examiner's Position

In the statement of the rejection, on page 3 of the Office Action, the Examiner asserted that KR 1999-73868 "shows most aspects" of the present invention, but acknowledged that KR 1999-73868 does not disclose a device including a second wiring layer provided over the substrate surface with a second insulator interposed therebetween. The Examiner merely concluded that the duplication of parts to obtain a multiple effect is considered an obvious modification, in order to have greater transmission capacity. This rejection is traversed as factually and legally erroneous.

Appellant's Position

Initially, Appellant incorporates herein the arguments previously advanced in traversing the imposed rejection of claims 18, 20 and 24 under 35 U.S.C. § 102 for lack of novelty as evidenced by KR 1999-73868. Claims 19, 21 and 23 are free from the applied art in view of their dependency from independent claim 18. Moreover, the separate patentability of claims 19, 21 and 23 is advocated.

It is well established that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The Examiner's rejection is based upon an unsupported generalization devoid of any factual basis. Therefore, the above described significant structural difference between the claimed semiconductor device and the semiconductor device of KR 1999-73868 undermines the Examiner's conclusion of obviousness under 35 U.S.C. § 103. Specifically, it is not apparent and the Examiner has not discharged the initial burden of providing any factual basis, as judicially required, upon which to predicate the determination that the duplication of parts would necessarily lead to greater transmission capacity. The Examiner bears the burden of establishing a prima facie case of obviousness and only if this burden is met does the burden of coming forward with rebuttal argument or evidence shift to the applicant. When the reference cited by the Examiner fails to establish a prima facie case of obviousness, the rejection is improper and should be overturned. *In re Deuel*, 34 USPQ 2d 1210, 1214 (Fed. Cir. 1995).

Appellant, therefore, submits that the imposed rejection of claims 19, 21 and 23 under 35 U.S.C. §103 for obviousness predicated upon KR 1999-73868 is not factually or legally viable and, hence, solicit reversal thereof.

IX. Conclusion

Based upon the arguments submitted supra, Appellant submits that the Examiner's rejections under 35 U.S.C. §§ 102 and 103 are factually and legally erroneous. Appellant, therefore, solicits the Honorable Board to reverse each of the Examiner's rejection under 35 U.S.C. §§ 102 and 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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CLAIMS APPENDIX

Claims 1-8 (Canceled)

9. (Withdrawn) A method of manufacturing a high-frequency semiconductor device comprising the steps of:

(A) preparing a semiconductor substrate having a main surface;

(B) depositing a first conductor layer to cover said main surface of said semiconductor substrate;

(C) flattening an upper surface of said first conductor layer;

(D) forming a first insulating film on said upper surface of said first conductor layer thus flattened;

(E) depositing a first conductive film on said first insulating film;

(F) forming a second insulating film on said first conductive film;

(G) patterning said first conductive film and said second insulating film, thereby forming a first wiring and a first upper insulating film covering an upper surface thereof; (H) depositing a third insulating film to cover said upper surface of said first conductor layer in such a thickness as to bury said first upper insulating film therein;

(I) removing said third insulating film to leave, as a first side wall, a portion covering side surfaces of said first wiring and said first upper insulating film;

(J) removing said first insulating film to leave portions covered with said first wiring and said first side wall, simultaneously with said step (I) or after said step (I);

(K) depositing a second conductor layer to cover said upper surface of said first conductor layer in such a thickness as to bury said first upper insulating film therein; and (L)

flattening an upper surface of said second conductor layer to maintain such a configuration that said first upper insulating film is buried.

10. (Withdrawn) A method of manufacturing a high-frequency semiconductor device comprising the steps of:

(A) preparing a semiconductor substrate having a main surface;

(B) depositing a first conductor layer to cover said main surface of said semiconductor substrate;

(C) flattening an upper surface of said first conductor layer;

(D) forming a first insulating film on said upper surface of said first conductor layer thus flattened;

(E) depositing a first sacrificial layer on said first insulating film;

(F) selectively forming, in said first sacrificial layer, a trench penetrating from an upper surface to a lower surface thereof;

(G) depositing a conductive material to fill in said trench;

(H) flattening said upper surface of said first sacrificial layer and an upper surface of said conductive material, thereby forming a first wiring of said conductive material;

(I) forming a second insulating film on said upper surface of said first sacrificial layer and an upper surface of said first wiring;

(J) removing said second insulating film to leave, as a first upper insulating film, a portion provided on said first wiring;

(K) removing said first sacrificial layer;

(L) depositing a third insulating film to cover said upper surface of said first conductor layer in such a thickness as to bury said first upper insulating film therein;

(M) removing said third insulating film to leave, as a first side wall, a portion covering side surfaces of said first wiring and said first upper insulating film;

(N) removing said first insulating film to leave portions covered with said first wiring and said first side wall, simultaneously with said step (M) or after said step (M); (O) depositing a second conductor layer to cover said upper surface of said first conductor layer in such a thickness as to bury said first upper insulating film therein; and (P) flattening an upper surface of said second conductor layer to maintain such a configuration that said first upper insulating film is buried.

11. (Withdrawn) The method of manufacturing a high-frequency semiconductor device according to claim 9, wherein said step (B) includes the steps of:

(B1) forming a fourth insulating film on said main surface;

(B2) forming a second conductive film on said fourth insulating film;

(B3) forming a fifth insulating film on said second conductive film;

(B4) patterning said second conductive film and said fifth insulating film, thereby forming a second wiring and a second upper insulating film covering an upper surface thereof;

(B5) depositing a sixth insulating film to cover said main surface of said semiconductor substrate in such a thickness as to bury said second upper insulating film therein;

(B6) removing said sixth insulating film to leave, as a second side wall, a portion covering side surfaces of said second wiring and said second upper insulating film;

(B7) removing said fourth insulating film to leave portions covered with said second wiring and said second side wall, simultaneously with said step (B6) or after said step (B6); and

(B8) depositing said first conductor layer to cover said main surface of said semiconductor substrate in such a thickness as to bury said second upper insulating film therein; and

said step (C) includes the step of:

(C1) flattening said upper surface of said first conductor layer to maintain such a configuration that said second upper insulating film is buried.

12. (Withdrawn) The method of manufacturing a high-frequency semiconductor device according to claim 10, wherein said step (B) includes the steps of:

(B1) forming a fourth insulating film on said main surface;

(B2) forming a second conductive film on said fourth insulating film;

(B3) forming a fifth insulating film on said second conductive film;

(B4) patterning said second conductive film and said fifth insulating film, thereby forming a second wiring and a second upper insulating film covering an upper surface thereof;

(B5) depositing a sixth insulating film to cover said main surface of said semiconductor substrate in such a thickness as to bury said second upper insulating film therein;

(B6) removing said sixth insulating film to leave, as a second side wall, a portion covering side surfaces of said second wiring and said second upper insulating film;

(B7) removing said fourth insulating film to leave portions covered with said second wiring and said second side wall, simultaneously with said step (B6) or after said step (B6); and

(B8) depositing said first conductor layer to cover said main surface of said semiconductor substrate in such a thickness as to bury said second upper insulating film therein; and

said step (C) includes the step of:

(C1) flattening said upper surface of said first conductor layer to maintain such a configuration that said second upper insulating film is buried.

13. (Withdrawn) The method of manufacturing a high-frequency semiconductor device according to claim 9, further comprising the steps of:

(AA) selectively forming, in said first insulating film and said first conductor layer, a through hole penetrating from an upper surface of said first insulating film to a lower surface of said first conductor layer, after said step (D) and before said step (E);

(BB) forming a side insulating film covering a side wall surface of said through hole before said step (E); and

(CC) forming a conductive plug to fill in said through hole with said side insulating film interposed therebetween before said step (E),

said first conductive film being also deposited on said through hole to be connected to said conductive plug at said step (E), and

said first wiring being formed to be connected to said conductive plug by covering said through hole at said step (G).

14. (Withdrawn) The method of manufacturing a high-frequency semiconductor device according to claim 12, further comprising the steps of:

(AA) depositing a second sacrificial layer to cover said main surface of said semiconductor substrate in such a thickness as to bury said second upper insulating film therein, after said step (B7) and before said step (B8); and

(BB) patterning said second sacrificial layer to leave a part thereof as a columnar portion before said step (BB),

said first conductor layer being deposited to cover said main surface of said semiconductor substrate in such a thickness as to bury said second upper insulating film therein at said step (B8), and

an upper surface of said columnar portion and said upper surface of said first conductor layer being flattened to maintain such a configuration that said second upper insulating film is buried at said step (Cl), and said method further comprising the steps of: (CC) removing said columnar portion, thereby forming a through hole in said first conductor layer after said step (C1) and before said step (D);

(DD) forming a side insulating film to cover a side wall surface of said through hole after said step (CC) and before said step (D); and

(EE) forming a conductive plug to fill in said through hole with said side insulating film interposed therebetween before said step (D),

said step (D) including the steps of:

(D1) forming said first insulating film on said upper surface of said first conductor layer which is flattened and over said through hole; and

(D2) selectively removing said first insulating film such that at least a part of an upper surface of said conductive plug is exposed,

said first sacrificial layer being deposited on an exposed surface of said conductive plug as well as on said first insulating film at said step (E),

said trench being formed such that said exposed surface of said conductive plug is exposed at said step (F), and said

conductive material being deposited to be connected to said exposed surface of said conductive plug at said step (G).

15. (Withdrawn) The method of manufacturing a high-frequency semiconductor device according to claim 14, wherein at least an upper surface portion of said fifth insulating film and said sixth insulating film are formed of the same material and said second sacrificial layer is formed of another material different therefrom.

16. (Withdrawn) The method of manufacturing a high-frequency semiconductor device according to claim 10, wherein at least an upper surface portion of said second insulating film and said third insulating film are formed of the same material.

17. (Canceled)

18. (Previously Presented) A high-frequency semiconductor device comprising:

a semiconductor substrate having a main surface;

a first wiring provided over said main surface of said semiconductor substrate; and

a grounding conductor layer continuously covering a periphery of said first wiring with a first insulator interposed therebetween in a section crossing a direction of extension of said first wiring, wherein said grounding conductor layer transmits a grounding potential and said grounding conductor layer includes a first portion constituted by only one unit covering an upper surface and two side surfaces of said first wiring and a second portion covering a bottom surface of said first wiring.

19. (Previously Presented) The high-frequency semiconductor device according to claim 18, further comprising a second wiring provided over said main surface of said semiconductor substrate with an insulating film interposed therebetween,

said grounding conductor layer continuously covering upper and side surfaces of said second wiring with a second insulator interposed therebetween in a section crossing a direction of extension of said second wiring and being connected to said semiconductor substrate.

20. (Previously Presented) The high-frequency semiconductor device according to claim 18, wherein an upper surface of said grounding conductor layer is flat.

21. (Previously Presented) The high-frequency semiconductor device according to claim 19, wherein said grounding conductor layer continuously covers a periphery of said second wiring in cooperation with said semiconductor substrate with said second insulator and said insulating film interposed therebetween in said section crossing said direction of extension of said second wiring.

22. (Previously Presented) The high-frequency semiconductor device according to claim 18,

wherein said first wiring is electrically connected to said semiconductor substrate through a conductor plug filled in a through hole selectively formed in said grounding conductor layer with a side insulating film interposed therebetween in a part taken in said direction of extension of said first wiring.

23. (Previously Presented) The high-frequency semiconductor device according to claim 19, wherein a portion of said second insulator which covers said upper and side surfaces of said second wiring and is provided in contact with said grounding conductor layer is formed of the same material.

24. (Previously Presented) The high-frequency semiconductor device according to claim 18, wherein a portion of said first insulator which covers upper and side surfaces of said first wiring and is provided in contact with said grounding conductor layer is formed of the same material.